IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant:	Anderson, et al	Examiner:	Lesniewski, Victor D
Filed:	2/7/2001	Art Unit:	2152

Docket No. : TI-30831
Customer No. : 23494
For: MULTI-PROCESSOR SYSTEM VERIFICATION CIRCUITRY

APPELLANTS' BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant respectfully present this brief in support of their appeal of the final rejection of the claims in this case. The Notice of Appeal was filed on August 17, 2006. A fee for filing this brief in support the appeal is submitted herewith.

i. Real party in interest

The real party in interest in this application is Texas Instruments Incorporated.

ii. Related Appeals and Interferences

The undersigned is aware of no appeals or interferences which will directly affect or have a bearing on, or be directly affected by, the Board's decision in this appeal.

iii. Status of claims

Claims 1 through 20 were finally rejected in the Office Action of April 17, 2006 and are the subject of the present appeal.

iv. Status of amendments

No amendments were filed after the Office Action of April 17, 2006. Therefore, the claims on appeal in this case are identical with those finally rejected.

v. *Summary of claimed subject matter*

A. *Overview*

This inventive claimed subject matter relates to debugging a slave processor subsystem independent of the implementation of the master processor. A verification interface on the slave processor selectively passes system memory accesses either to a system memory or to a shared memory (accessible to both the master processor and the slave processor) responsive to a signal specifying a normal (operating) mode or a verification (testing) mode. While in normal mode, accesses directed towards the system memory access are passed to the system memory. While in verification mode, accesses directed towards the system memory are passed to the shared memory.

B. *Relating Overview to Independent Claims*

Independent claims 1, 8 and 13 are pending in this appeal. Each is set forth below with reference numbers of examples, in parenthesis, and with reference to support in the text and drawings of the Specification and consistent with the Overview provided above.

1. *Claim 1*

Claim 1 is directed to a processing device (40) including a master processor (16), a system memory (20) and a slave processor subsystem (14). The slave processor subsystem (14) includes a slave processor (26), a shared memory (24) accessible by the master processor (16) and the slave processor (26), an external memory interface (30) allowing the slave processor (26) to access the system memory (20), circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device or verification mode for testing the processing device (40) and a verification interface (42). The verification interface (42)[1] selectively passes system memory accesses either to the system memory (20) or the shared memory (24) responsive to the signal.

[1] Page 7, line 25 through page 9, line 22.

Accesses directed towards the system memory (20) are passed to the system memory (20) in a normal mode and accesses directed towards the system memory (20) are passed to the shared memory (24) in a verification mode.

This aspect of the invention provides significant advantages over the prior art. First, debugging the slave processor subsystem may be performed without understanding the implementation of the master processor subsystem. Second, extraneous interactions are isolated from the slave processor system during verification procedures. Third, the external memory interface can be production tested at operating speed in the same way as an application is actually executed in the field, thereby increasing the fault coverage and capability for performance testing of the slave subsystem.

2. Claim 8

Claim 8 is a method of verification of a processing device (40) including a master processing subsystem (12) including a master processor (16) and a system memory (20) and a slave processor subsystem (14) including a slave processor (26), a shared memory (24) accessible by the master processor (16) and the slave processor (26), an external memory interface (30) for accessing the system memory (20) and a shared memory (24) accessible by the master processor and the slave processor. A signal is received specifying either a normal mode for normal operation of the processing device or verification mode for testing the processing device (40) and a verification interface (42). System memory accesses are selectively passed to the system memory (20) in a normal mode and system memory accesses are selectively passed to the shared memory (24) in a verification mode[2].

The method of claim 8 provides the same benefits as stated for the method of claim 1.

[2] Page 7, line 25 through page 9, line 22.

3. Claim 13

Claim 13 is directed to a processing device (40) including a master processor (16), a system memory (20) and a slave processor subsystem (14). The slave processing subsystem (14) includes one or more slave processors (26), a shared memory (24) accessible by the master processor (16) and the slave processors (26), an external memory interface (30) allowing the slave processor (26) to access the system memory (20), circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device or verification mode for testing the processing device (40) and a verification interface (42). The verification interface (42)[3] selectively passes system memory accesses either to the system memory (20) or the shared memory (24) responsive to the signal. Accesses directed towards the system memory (20) are passed to the system memory (20) in a normal mode and accesses directed towards the system memory (20) are passed to the shared memory (24) in a verification mode.

The processing device of claim 13 provides the same benefits as stated for the method of claim 1.

[3] Page 7, line 25 through page 9, line 22.

vi. Grounds of rejection to be reviewed on appeal

A. Rejections Under 35 U.S.C. § 103

The Examiner has rejected claims 1, 4-6, 8, 10, 11, 13, 14 and 17-19 under 35 U.S.C. §103(a) as being unpatentable over DeRoo in view of U.S. Pat. No. 6,016,525 to Corrigan. The Examiner has rejected claims 2, 3, 7, 9, 12, 15, 16 and 20 under 35 U.S.C. §103(a) as being unpatentable over DeRoo in view Corrigan and further in view of U.S. Pat. No. 5,887,146 to Baxter.[4]

With regard to independent claims 1 and 8, the Examiner states that DeRoo shows a processing device comprising: a master processor; a system memory; a slave processor subsystem including: a slave processor; a shared memory accessible by the master processor and the slave processor (citing DeRoo, column 2, lines 13-31), an external memory interface allowing the slave processor to access the system memory (citing DeRoo, column 8, lines 21-30); circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device (citing DeRoo, column 20, lines 15-25) or a verification mode for testing the processing device (citing DeRoo, column 19, lines 29-38). The Examiner admits that DeRoo does not explicitly show selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to the system memory in a normal mode and wherein accesses directed towards the system memory are passed to the shared memory in a verification mode. However, the Examiner states that Corrigan shows a verification interface for selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to the system memory in a normal mode and wherein accesses directed towards the system memory are passed to the shared memory in a

[4] Office action of April 17, 2006, page 2.

verification mode (citing Corrigan, column 2, line 50 through column 3, line 31).[5] The Examiner further states that the combination of DeRoo and Corrigan clearly shows the enablement of a loopback operation during which a data transfer to the secondary bus is redirected to the shared memory interface and that the loopback mode is a verification mode as it improves the testability of the circuit by using the shared memory interface to test downstream transactions (citing Corrigan, Figure 2 and column 5, line 64 through column 6, line 27). Further, the Examiner states that the downstream transactions in Corrigan are addressed as though normally destined for the secondary PCI bus, but in loopback (or verification) mode the configuration parameters allow the transaction to be directed to the shared memory (citing Corrigan, column 2, line 50 through column 3, line 31 and column 5, line 64 through column 6, line 27).[6] The Examiner states that Corrigan writes data intended for an external system memory to an internal shared memory, as one PCI bus sends a write transaction to a second PCI bus but has it redirected to shared memory in a test mode.[7]

With regard to dependent claim 2, the Examiner states Baxter shows a slave processor subsystem which includes a cache memory coupled to the external memory controller and the slave processor (citing Baxter, column 4, line 67 through column 5, line 21).[8]

With regard to dependent claims 3 and 9, the Examiner states that Baxter shows a verification interface including a protocol translator for translating between a first protocol associated with memory accesses of the system memory and a second protocol associated with memory accesses of the shared memory (citing Baxter, column 5, lines 34-37).[9]

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[5] Office Action of September 21, 2005, page 4.
[6] Office Action of April 17, 2006, page 3.
[7] Office Action of April 17, 2006, pages 3-4.
[8] Office Action of September 21, 2005, page 7.
[9] Office Action of September 21, 2005, page 7.

With regard to dependent claims 4, 10 and 11, the Examiner states that DeRoo shows a verification interface comprising multiplexing circuitry for passing data to the external memory interface from either the system memory or the shared memory responsive to whether the verification interface is in a normal mode or a verification mode (citing DeRoo, column 82, lines 7-39).[10]

With regard to dependent claim 5, the Examiner states DeRoo shows a control interface coupled between the master processor and the shared memory (citing DeRoo, column 2, lines 18-24).[11]

With regard to dependent claim 6, the Examiner states that DeRoo shows multiplexing circuitry comprising first multiplexing circuitry and further comprising second multiplexing circuitry for passing control signals to the control interface from either the master processor or the external memory interface responsive to whether the verification interface is in a normal mode or a verification mode (DeRoo, column 83, lines 28-44).[12]

With regard to dependent claims 7 and 12, the Examiner states that Baxter shows a protocol translator for translating between a first protocol associated with memory accesses of the system memory and a second protocol associated with memory accesses of the shared memory (citing Baxter, column 5, lines 34-37).[13]

With regard to independent claim 13, the Examiner states that DeRoo shows a master processor; a system memory; a slave processor subsystem including: one or more slave processors; a shared memory accessible by the master processor and the slave processors (citing DeRoo, column 2, lines 13-31); circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device (citing DeRoo,

[10] Office Action of September 21, 2005, page 4.
[11] Office Action of September 21, 2005, page 4.
[12] Office Action of September 21, 2005, page 5.
[13] Office Action of September 21, 2005, page 8.

column 20, lines 15-25) or verification mode for testing the processing device (citing DeRoo, column 19, lines 29-38); and a system memory interface allowing the slave processors to access the system memory (citing DeRoo, column 8, lines 21-30) and Corrigan shows a verification interface for selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to the system memory in a normal mode and wherein accesses directed towards the system memory are passed to the shared memory in a verification mode (citing Corrigan, column 2, line 50 through column 3, line 31).[14]

With regard to dependent claim 14, the Examiner states that DeRoo shows a system memory interface comprising respective external memory interfaces associated with each slave processor and a memory arbiter for arbiting between memory accesses generated by each of the external memory interfaces (citing DeRoo, column 2, lines 13-31).[15]

With regard to dependent claim 15, the Examiner states that Baxter shows a slave processor subsystem further including cache memories associated with each of the slave processors (citing Baxter, column 4, line 67 through column 5, line 21).[16]

With regard to dependent claim 16, the Examiner states that Baxter shows a verification interface including a protocol translator for translating between a first protocol associated with memory accesses of the system memory and a second protocol associated with memory accesses of the shared memory (citing Baxter, column 5, lines 34-37).[17]

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[14] Office Action of September 21, 2005, page 5.
[15] Office Action of September 21, 2005, pages 5-6.
[16] Office Action of September 21, 2005, page 8.
[17] Office Action of September 21, 2005, page 8.

With regard to dependent claim 17, the states that DeRoo shows a verification interface comprising multiplexing circuitry for passing data to the system memory interface from either the system memory or the shared memory responsive to whether the verification interface is in a normal mode or a verification mode (citing DeRoo, column 82, lines 7-39).[18]

With regard to dependent claim 18, the Examiner states that DeRoo shows a control interface coupled between the master processor and the shared memory (citing DeRoo, column 2, lines 18-24).[19]

With regard to dependent claim 19, the Examiner states that DeRoo shows multiplexing circuitry comprises first multiplexing circuitry and further comprising second multiplexing circuitry for passing control signals to the control interface from either the master processor or the system memory interface responsive to whether the verification interface is in a normal mode or a verification mode (citing DeRoo, column 83, lines 28-44).[20]

With regard to dependent claim 20, the Examiner states that Baxter shows a protocol translator for translating between a first protocol associated with memory accesses of the system memory and a second protocol associated with memory accesses of the shared memory (citing Baxter, column 5, lines 34-37).[21]

[18] Office Action of September 21, 2005, page 6.
[19] Office Action of September 21, 2005, page 6.
[20] Office Action of September 21, 2005, page 6.
[21] Office Action of September 21, 2005, page 8.

vii. Argument

It is axiomatic, in the patent law, that a *prima facie* obviousness determination of patent claims requires teachings from the prior art itself to appear to have suggested the claimed subject matter to a person of ordinary skill in the art.[22] If the Examiner fails to establish a *prima facie* case, the rejection is improper and should be overturned on appeal.[23] Appellants respectfully submit that the final rejection fails to meet this standard. Instead, the teachings of the applied prior art, properly interpreted, fall short of the requirements of each of the claims, and there is no suggestion from the prior art to modify those teachings in such a manner as to reach the claims on appeal in this case.

A. Rejections Under 35 U.S.C. § 103

Before discussing the specifics of the various rejections, it is beneficial to describe the general nature of the cited references.

The DeRoo reference is directed to a multiprocessing computer system with multiplexed address and data paths from multiple CPUs to a single storage device. The paths to the storage device are controlled by an arbitration circuit that allows one CPU to always have the highest priority. As noted above, the Examiner agrees that DeRoo does not show a verification interface. DeRoo does not discuss a normal mode and a verification mode, nor does DeRoo discuss circuitry providing access to different memories responsive to different modes; specifically, DeRoo has no teaching of re-directing memory accesses to a system memory to a shared memory that is part of the slave processor subsystem.

The Corrigan reference was used by the Examiner to provide teaching for the verification interface. Corrigan describes a bridge circuit for providing communication between a primary and a secondary PCI bus. The Corrigan device has an internal

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[22] *In re Rijckaert*, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993).
[23] *Id.*

loopback mode for testing the operation of the bridge circuit. The Examiner claims that the disclosure of the loopback testing mode of Corrigan shows the verification interface as claimed.

The Baxter reference is directed to a multiprocessing system. This reference is used by the Examiner to show various aspects of the dependent claims, including a cache memory and a protocol translator.

1. Claims 1, 8 and 13

The Examiner contends that DeRoo shows all aspects of these claims, except of those relating to the verification interface. As specified in claim 1, the verification interface selectively passes "memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to said system memory in a normal mode and wherein accesses directed towards the system memory are passed to said shared memory in a verification mode."

Applicant cannot agree with the Examiner's characterization of DeRoo. While DeRoo discusses multiple processors accessing a shared memory, the structure set forth in the claims is much more specific. First, there must be a master processor and a slave processor subsystem, where the slave processor subsystem includes a shared memory accessible to the master processor and slave processor. Further, the slave processor has an external memory interface allowing access to the system memory.

DeRoo shows multiple processors which have prioritized access to a shared memory. The shared memory (704) is not part of a slave processor subsystem.

Further, the DeRoo reference does not show circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device or verification mode for testing the processing device. The Examiner appears to contend that the ISOLATE signal specifies a normal or test mode. The DeRoo reference defines the

ISOLATE signal as follows: "[a]n isolate signal is an active low input signal to tristate certain signals on the SCPI 28 in the event that the SCP 26 and SCPI 28 are used in a manner where the rest of the system is not powered, for example, during battery charging of a portable battery powered converter. Tristating the pins identified in TABLE IV below can avoid problems to the SCP 26."[24] While the ISOLATE signal can be used in test mode[25], it is clearly not indicative of a normal/test mode, since it can be used at other times, such as during battery charging, as noted above.

The Examiner claims that the verification interface is shown in Corrigan. Applicant disagrees with the Examiner's contention. Specifically, Corrigan does not show a verification interface where accesses *directed towards the system memory* are passed to said system memory in a *normal* mode and wherein accesses *directed towards the system memory* are passed to said *shared* memory in a *verification* mode.

Specifically, Corrigan shows the ability to access a shared memory 202 in one of two ways. First, the shared memory 202 can be accessed in a normal fashion over the primary PCI bus 252. Second the shared memory 202 can be accessed over the following path: PCI Bridge (Primary interface) 2, pad flow circuit 6, pad 8, pad flow circuit 6 (a second time), shared memory bridge 4, and shared memory bus 250. The purpose of using the second path is to test the circuitry in the PCI bridge 2 and shared memory bridge 4.

More specifically, the PCI bridge 2 in Corrigan allows devices on the secondary PCI bus 256 to communicate with devices on the primary PCI bus 252, and vice versa (col. 4, lines 135-54). The shared memory bridge 4 allows device on the secondary PCI bus 256 to read and write to the shared memory 202 (col. 5. lines 10-20).

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[24] DeRoo, column 17, lines 10-16.
[25] DeRoo, column 19, lines 35-38.

Each bridge 2 and 4 recognizes data transfers requiring its attention based on the address supplied in the transfer request. The PCI bridge 2 uses an address range specified in the secondary address register 12 and the shared memory bridge 4 uses an address range specified in the shared memory address register 14. If the address ranges in these two registers overlap (loopback mode), and a transfer request on the primary PCI bus 252 specifies an address within the overlapping range, the following will occur: (1) the PCI bridge 2 will see this as a request to access a device on the secondary bus 256 through the PCI bridge 2; the request will thus be translated and placed on the secondary bus 256 and (2) the shared memory bridge 4 will see the translated request as a request to access shared memory 202, and will thus translate the request back to the protocol used on the primary PCI bus to access the shared memory (col. 6, lines 6-27). This path is shown in Figures 2 and 3 of Corrigan.

Accordingly, Corrigan shows two *paths* available for a device on the primary bus 252 to access a *single* shared memory 202 which exists *external to the bridge circuit*. A device on the primary PCI bus can thus access the shared memory either directly over the primary PCI bus or indirectly via the secondary PCI bus and the two bridges 2 and 4. Corrigan does *not*, however, teach selectively passing memory accesses intended for a *system* memory to either a *system* memory or an *internal shared* memory responsive to a verification mode signal. No system memory is discussed in Corrigan. Corrigan states "[t]he *downstream transactions* are addressed as though normally destined for the *secondary PCI bus*."[26] A transaction destined for a secondary PCI bus is quite different than a memory access to a system memory.

In short, the Corrigan device does not pass a system memory accesses to a shared memory access; only shared memory accesses are passed to the shared memory. The only difference in the direct mode or the loopback mode in Corrigan is the *path taken to*

[26] Corrigan, column 6, lines 8-10.

reach the shared memory. Loopback mode in Corrigan does not affect the memory to which a memory access is directed.

It should be further noted that Corrigan also does not show circuitry for receiving a signal for indicating a test or normal mode, nor does it show a slave processor subsystem with a shared memory.

The Examiner provides no insight on how combining DeRoo with Corrigan would yield the present invention. The bridge circuit 206 is for coupling two buses together. External to the bridge circuit 206, a primary bus master 200 can initiate downstream transactions on the primary PCI bus 252.[27] At best, combining DeRoo with Corrigan would only result in a device having a master processor that could access a single memory *using one of two possible paths*. Any access request intended for the shared memory would eventually access the shared memory regardless of whether the device was in loopback mode – the only difference would be which path was used to get to the shared memory. *Corrigan does not provide for a memory access to a system memory to be passed instead to another, internal, memory and DeRoo does not provide for a slave processor subsystem having a shared memory and circuitry for receiving a signal indicating either a test or verification mode*. Thus, it would not be able to provide the debugging capabilities of the present invention, because it does not have the capability to selectively re-direct memory access requests intended for the system memory to a shared memory in the slave processor subsystem while in a verification mode. In the present invention, a slave processor that normally writes to an external system memory associated with a master processor can write (in verification mode) to an internal shared memory. Thus, in verification mode in the present invention, the slave processor subsystem can be completely isolated from the master processor subsystem. This is not true of the combination of DeRoo and Corrigan.

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[27] Corrigan, column 6, lines6-10.

Accordingly, Appellant submits that independent claims 1, 8 and 13 are novel and unobvious over the teachings of DeRoo and Corrigan.

For reasons stated above in connection with independent claims, Appellant submits that dependent claims 2-7, 9-12 and 14-20 are novel and unobvious over the teachings of DeRoo, Corrigan and Baxter as well.

viii. Claims appendix

Listing of Claims:

1. A processing device comprising:

a master processor;

a system memory;

a slave processor subsystem including:

a slave processor;

a shared memory accessible by said master processor and said slave processor;

an external memory interface allowing said slave processor to access said system memory;

circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device or verification mode for testing the processing device; and

a verification interface for selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to said system memory in a normal mode and wherein accesses directed towards the system memory are passed to said shared memory in a verification mode.

2. The processing device of claim 1 wherein said slave processor subsystem further includes a cache memory coupled to said external memory controller and said slave processor.

3. The processing device of claim 1 wherein said verification interface includes a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory.

4. The processing device of claim 1 wherein said verification interface comprises multiplexing circuitry for passing data to said external memory interface from either said system memory or said shared memory responsive to whether said verification interface is in a normal mode or a verification mode.

5. The processing device of claim 4 and further comprising a control interface coupled between said master processor and said shared memory.

6. The processing device of claim 5 wherein said multiplexing circuitry comprises first multiplexing circuitry and further comprising second multiplexing circuitry for passing control signals to said control interface from either said master processor or said external memory interface responsive to whether said verification interface is in a normal mode or a verification mode.

7. The processing device of claim 6 and further comprising a protocol translator for translating between a first protocol associated with memory accesses of

said system memory and a second protocol associated with memory accesses of said shared memory.

8. A method of verification of a processing device including a master processor subsystem having a master processor and a system memory and a slave processor subsystem having a slave processor, a external memory interface for accessing said system memory, and a shared memory accessible by the master processor and slave processor, comprising the steps of:

receiving a signal for specifying a normal mode for normal operation of the processing device or a verification mode for testing the processing device;

selectively passing system memory accesses to said system memory in a normal mode; and

selectively passing system memory accesses to said shared memory in a verification mode.

9. The method of claim 8 and further comprising the step of translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory.

10. The method of claim 8 wherein said step of passing system memory accesses to said system memory comprises the step of enabling multiplexing circuitry to pass data to said external memory interface from said system memory when said verification interface is in said normal mode.

11. The method of claim 9 wherein said step of passing system memory accesses to said shared memory comprises the step of enabling multiplexing circuitry to pass data to said external memory interface from said shared memory when said verification interface is in said verification mode.

12. The method of claim 11 and further comprising a translating from a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory when said verification interface is in said verification mode.

13. A processing device comprising:

a master processor;

a system memory;

a slave processor subsystem including:

one or more a slave processors;

a shared memory accessible by said master processor and said slave processors;

circuitry for receiving a signal for specifying a normal mode for normal operation of the processing device or verification mode for testing the processing device;

a system memory interface allowing said slave processors to access said system memory; and

a verification interface for selectively passing system memory accesses either to the system memory or the shared memory responsive to the signal, wherein accesses directed towards the system memory access are passed to said system memory in a normal mode and wherein accesses directed towards the system memory are passed to said shared memory in a verification mode.

14. The processing device of claim 13 wherein said system memory interface comprises:

respective external memory interfaces associated with each slave processor; and

a memory arbiter for arbiting between memory accesses generated by each of said external memory interfaces.

15. The processing device of claim 13 wherein said slave processor subsystem further includes cache memories associated with each of said slave processors.

16. The processing device of claim 13 wherein said verification interface includes a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory.

17. The processing device of claim 13 wherein said verification interface comprises multiplexing circuitry for passing data to said system memory interface from either said system memory or said shared memory responsive to whether said verification interface is in a normal mode or a verification mode.

18. The processing device of claim 17 and further comprising a control interface coupled between said master processor and said shared memory.

19. The processing device of claim 18 wherein said multiplexing circuitry comprises first multiplexing circuitry and further comprising second multiplexing circuitry for passing control signals to said control interface from either said master processor or said system memory interface responsive to whether said verification interface is in a normal mode or a verification mode.

20. The processing device of claim 19 and further comprising a protocol translator for translating between a first protocol associated with memory accesses of said system memory and a second protocol associated with memory accesses of said shared memory.

ix. Evidence appendix

None.

x. Related proceedings appendix

None.

xi. Conclusion

For the foregoing reasons, Appellants respectfully submit that the final rejection of claims 1 through 20 is in error. Reversal of the rejection is respectfully requested.

Respectfully submitted,

/Alan Lintel/

Alan Lintel

Registry No. 32,478

Attorney for Appellants

Anderson, Levine & Lintel, L.L.P.
14785 Preston Road, Suite 650
Dallas, Texas 75254
(972) 664-9595